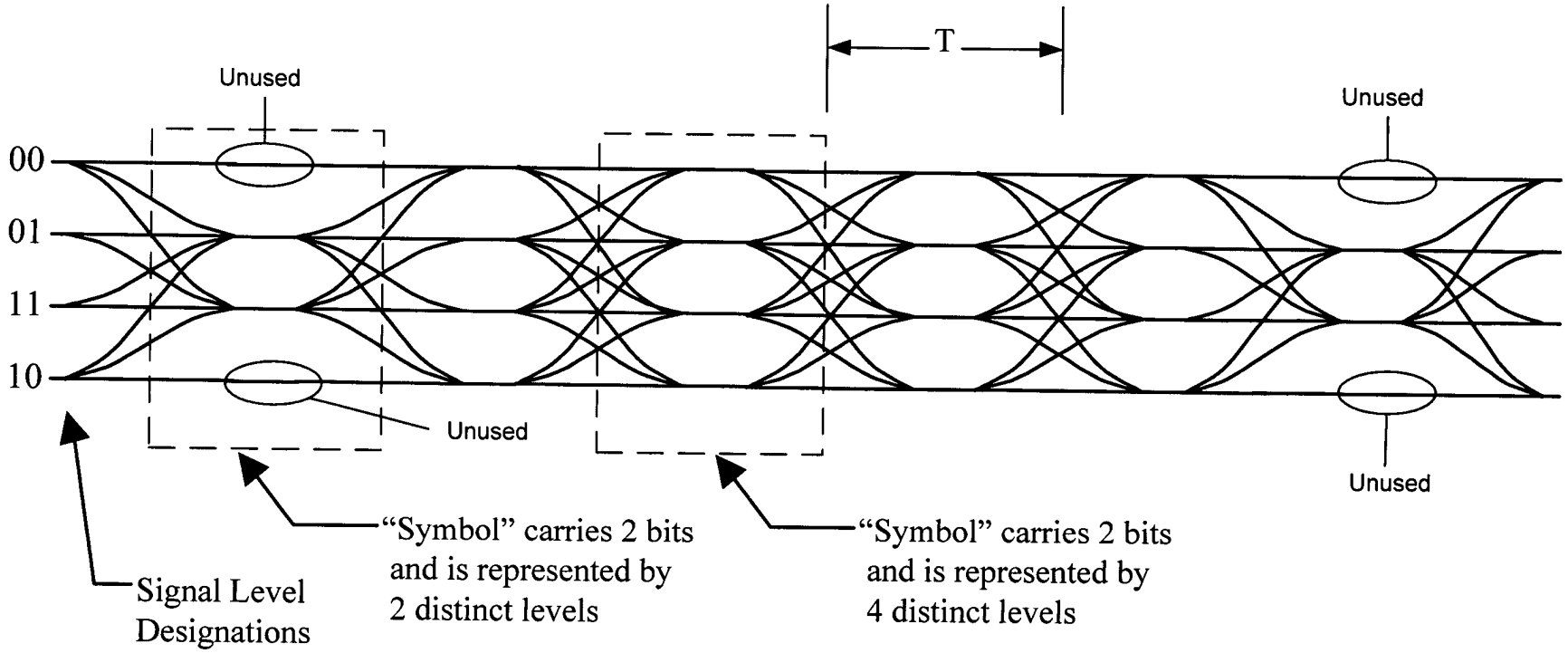
T
Unused
Unused
00
01
11
10
Unused
Unused
Signal Level Designations
"Symbol" carries 2 bits and is represented by 2 distinct levels
"Symbol" carries 2 bits and is represented by 4 distinct levels

Figure 1

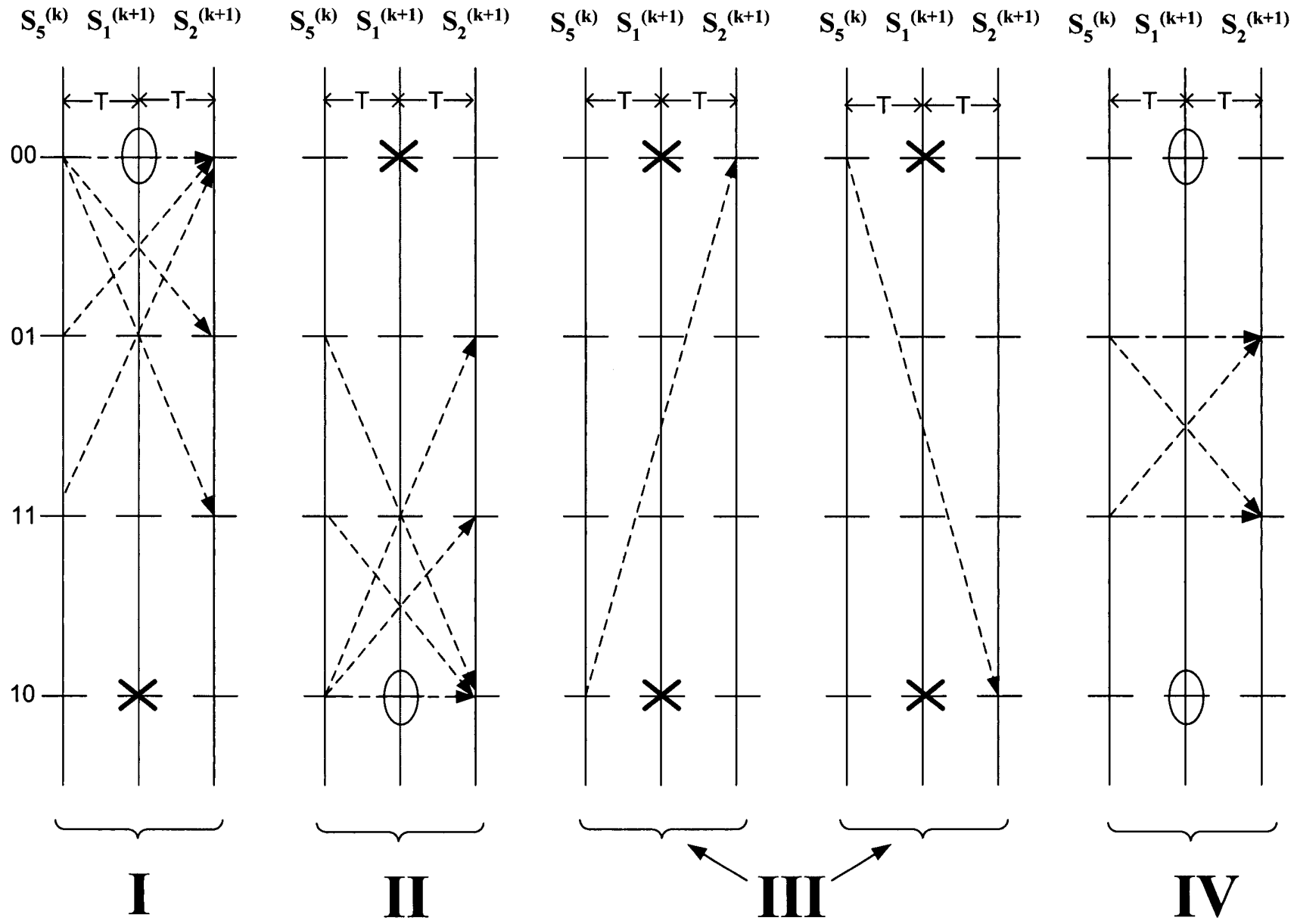

Figure 2

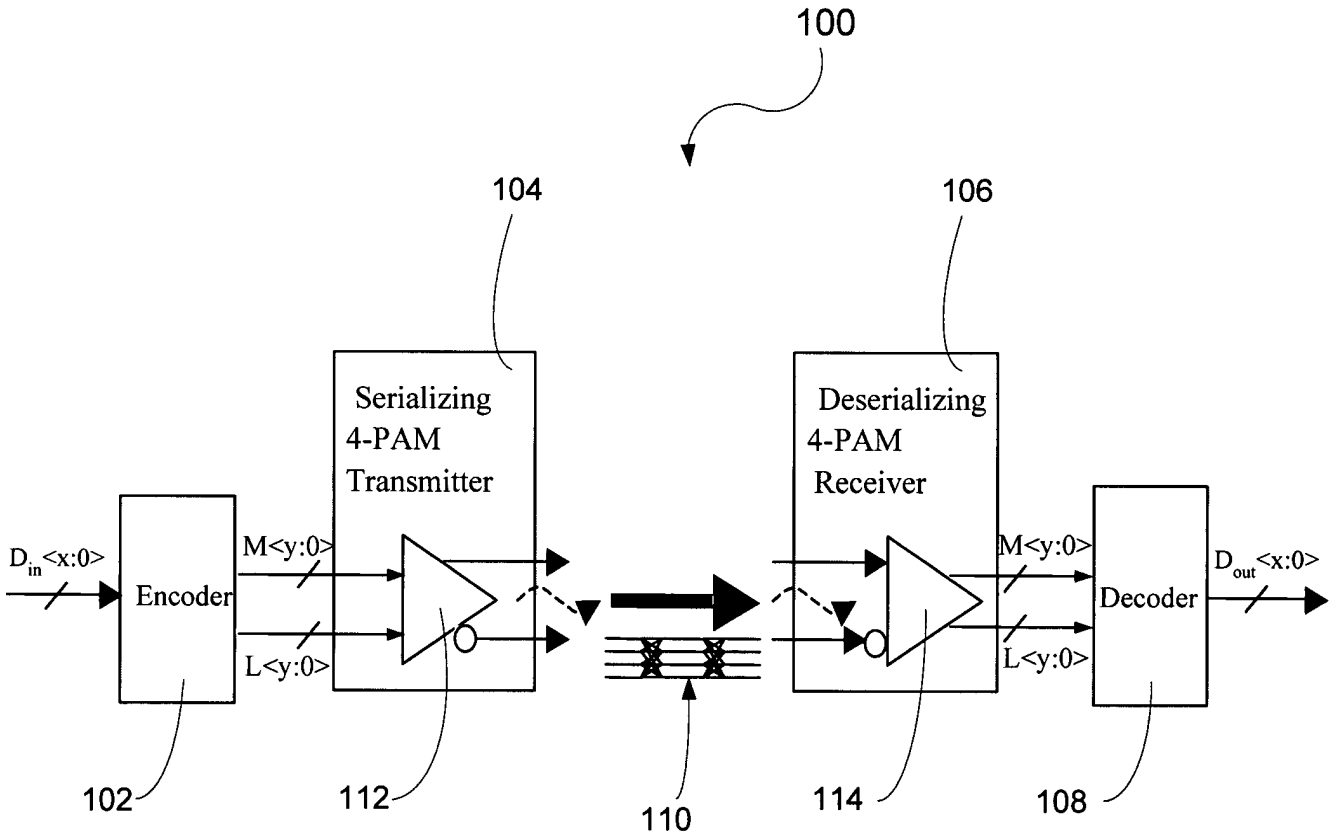
100
104
106
Serializing
4-PAM
Transmitter
Deserializing
4-PAM
Receiver
D_in<x:0>
Encoder
M<y:0>
L<y:0>
M<y:0>
L<y:0>
Decoder
D_out<x:0>
102
112
110
114
108

Figure 3

CASE I

Symbol Domain

Case I: $[(S_5^{(k)} = 3)\ \&\ (S_2^{(k+1)} = \pm 1 \text{ or } 3)]$ OR $[(S_5^{(k)} = \pm 1)\ \&\ (S_2^{(k+1)} = 3)]$

(a) if Case I & $(S_1^{(k+1)} = 1)$ → $S_1^{(k+1)} = 3$

(b) if Case I & $(S_1^{(k+1)} = -1)$ → $S_1^{(k+1)} = 3$

Bit Domain

Case I: $\left[(C_9^{(k)} = C_{10}^{(k)} = 0)\ \&\ [(C_3^{(k+1)} = C_4^{(k+1)} = 0) \text{ OR } (C_4^{(k+1)} = 1)]\right]$ OR $\left[(C_{10}^{(k)} = 1)\ \&\ (C_3^{(k+1)} = C_4^{(k+1)} = 0)\right]$

(a) if Case I & $(C_1^{(k+1)} = 0)\ \&\ (C_2^{(k+1)} = 1)$ → invert $C_2^{(k+1)}$

(b) if Case I & $(C_1^{(k+1)} = 1)\ \&\ (C_2^{(k+1)} = 1)$ → invert $C_1^{(k+1)}$ and $C_2^{(k+1)}$

$m1 = \text{Case I}\ \&\ (C_2^{(k+1)} = 1)$

Figure 4

CASE II

Symbol Domain

Case II: $[(S_5^{(k)} = -3)\ \&\ (S_2^{(k+1)} = \pm 1 \text{ or } -3)]$ OR $[(S_5^{(k)} = \pm 1)\ \&\ (S_2^{(k+1)} = -3)]$

(a) if Case II & $(S_1^{(k+1)} = -1)$ → $S_1^{(k+1)} = -3$

(b) if Case II & $(S_1^{(k+1)} = 1)$ → $S_1^{(k+1)} = -3$

Bit Domain

Case II: $\left[[(C_9^{(k)} = 1)\ \&\ (C_{10}^{(k)} = 0)]\ \&\ [(C_4^{(k+1)} = 1) \text{ OR } ((C_3^{(k+1)} = 1)\ \&\ (C_4^{(k+1)} = 0))]\right]$ OR $\left[(C_{10}^{(k)} = 1)\ \&\ [(C_3^{(k+1)} = 1)\ \&\ (C_4^{(k+1)} = 0)]\right]$

(a) if Case II & $(C_1^{(k+1)} = C_2^{(k+1)} = 1)$ → invert $C_2^{(k+1)}$

(b) if Case II & $\left[(C_1^{(k+1)} = 0)\ \&\ (C_2^{(k+1)} = 1)\right]$ → invert $C_1^{(k+1)}$ and $C_2^{(k+1)}$

m2 = Case II & $(C_2^{(k+1)} = 1)$

Figure 5

CASE IV

Symbol Domain

Case IV: $(S_5^{(k)} = \pm 1)$ & $(S_2^{(k+1)} = \pm 1)$

(a) if Case IV & $(S_1^{(k+1)} = 1)$ → $S_1^{(k+1)} = 3$

(a) if Case IV & $(S_1^{(k+1)} = -1)$ → $S_1^{(k+1)} = -3$

(b) if Case IV & $(S_1^{(k+1)} = 1)$ → $S_1^{(k+1)} = -3$

(b) if Case IV & $(S_1^{(k+1)} = -1)$ → $S_1^{(k+1)} = 3$

Bit Domain

Case IV: $(C_{10}^{(k)} = 1)$ & $(C_4^{(k+1)} = 1)$

(a) if Case IV & $(C_2^{(k+1)} = 1)$ → invert $C_2^{(k+1)}$

(b) if Case IV & $(C_2^{(k+1)} = 1)$ → invert $C_1^{(k+1)}$ and $C_2^{(k+1)}$

m4 = Case IV & $(C_2^{(k+1)} = 1)$

Figure 6

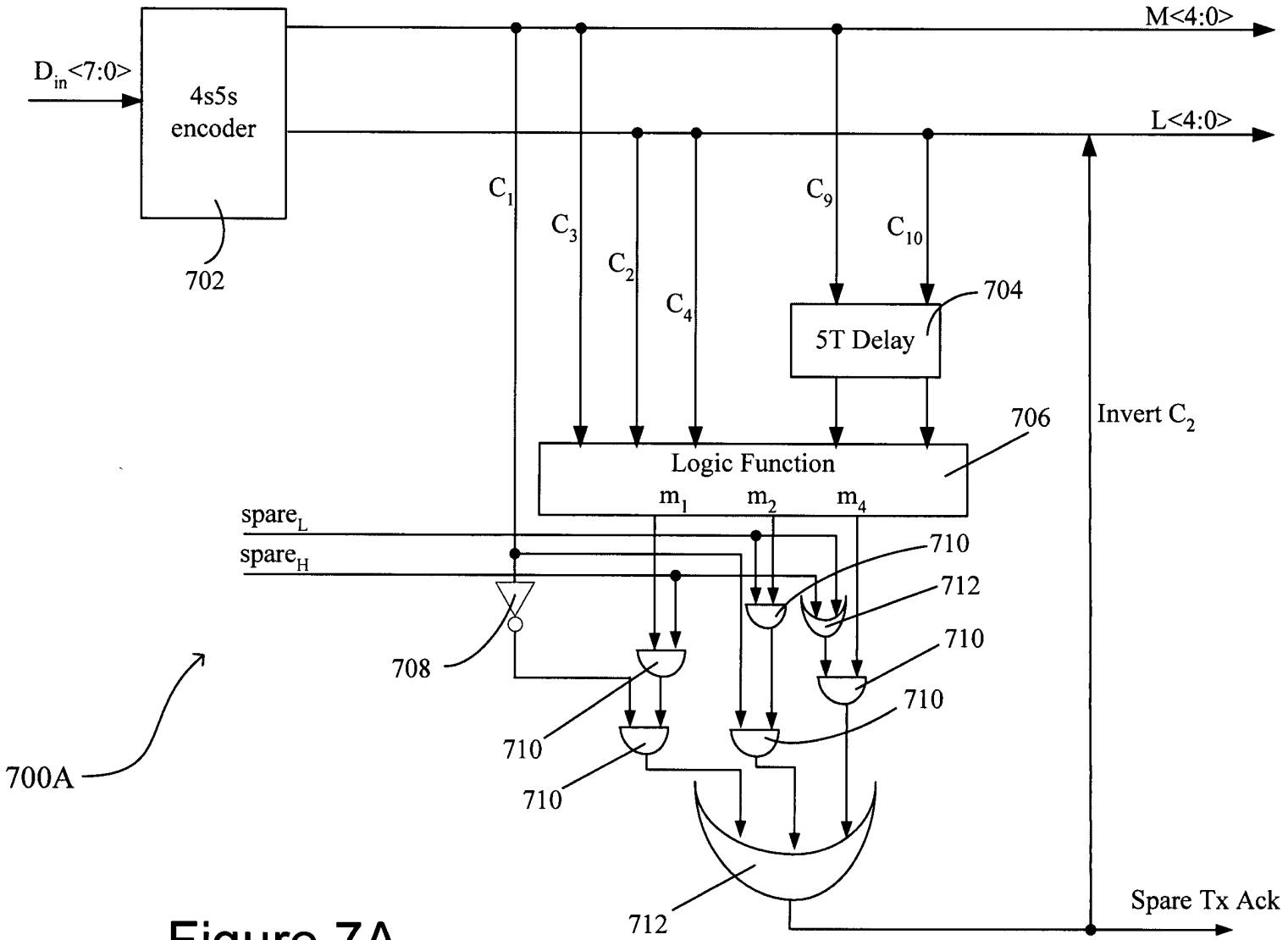
M<4:0>
L<4:0>
D_{in}<7:0>
4s5s encoder
702
C_1
C_3
C_2
C_4
C_9
C_{10}
704
5T Delay
706
Logic Function
m_1
m_2
m_4
Invert C_2
$spare_L$
$spare_H$
710
712
708
700A
Spare Tx Ack

Figure 7A

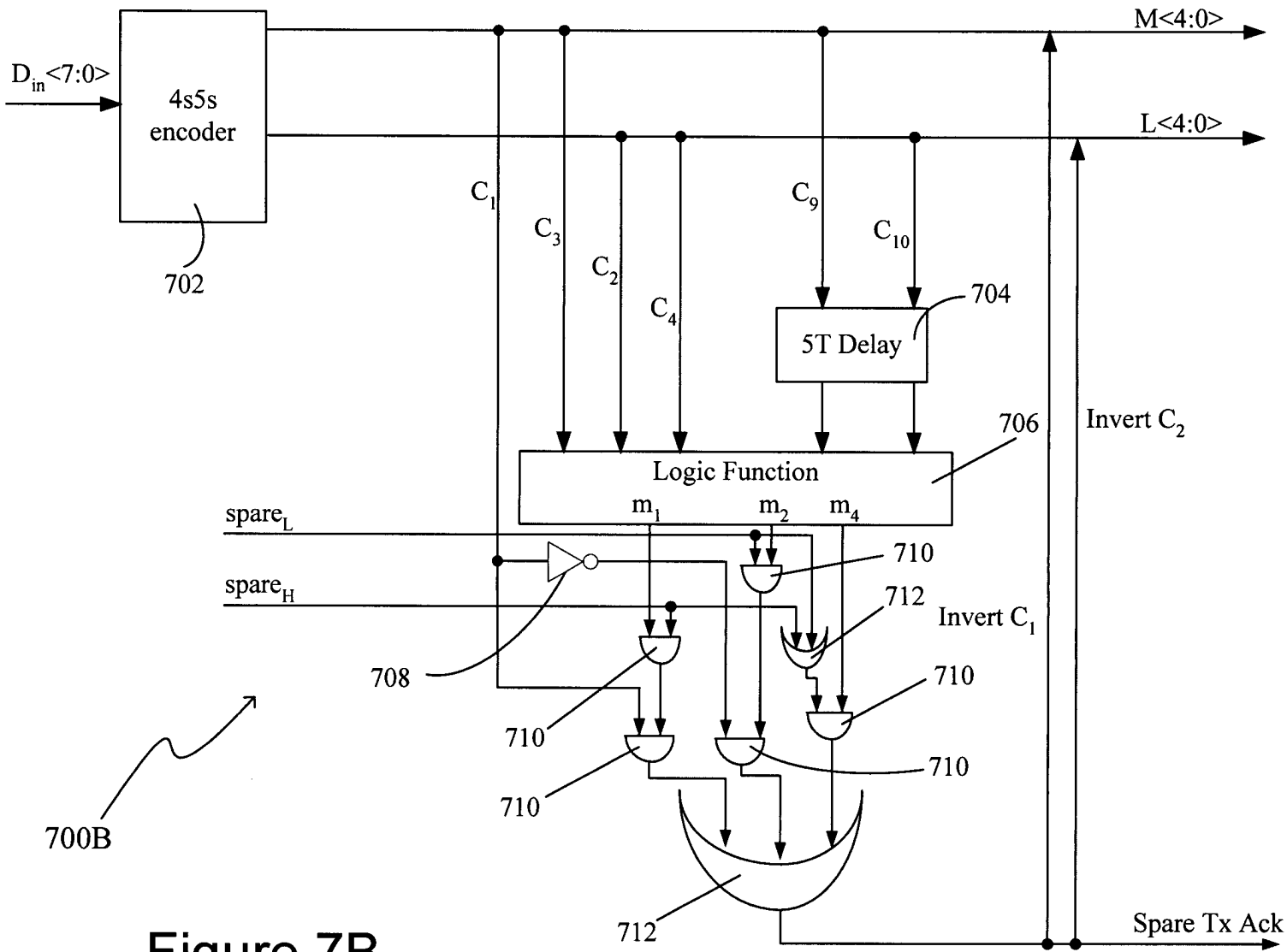
D_{in}<7:0>
4s5s
encoder
702
M<4:0>
L<4:0>
C_1
C_3
C_2
C_4
C_9
C_{10}
704
5T Delay
706
Logic Function
m_1
m_2
m_4
Invert C_2
$spare_L$
$spare_H$
710
712
Invert C_1
708
710
710
710
710
712
Spare Tx Ack
700B

Figure 7B

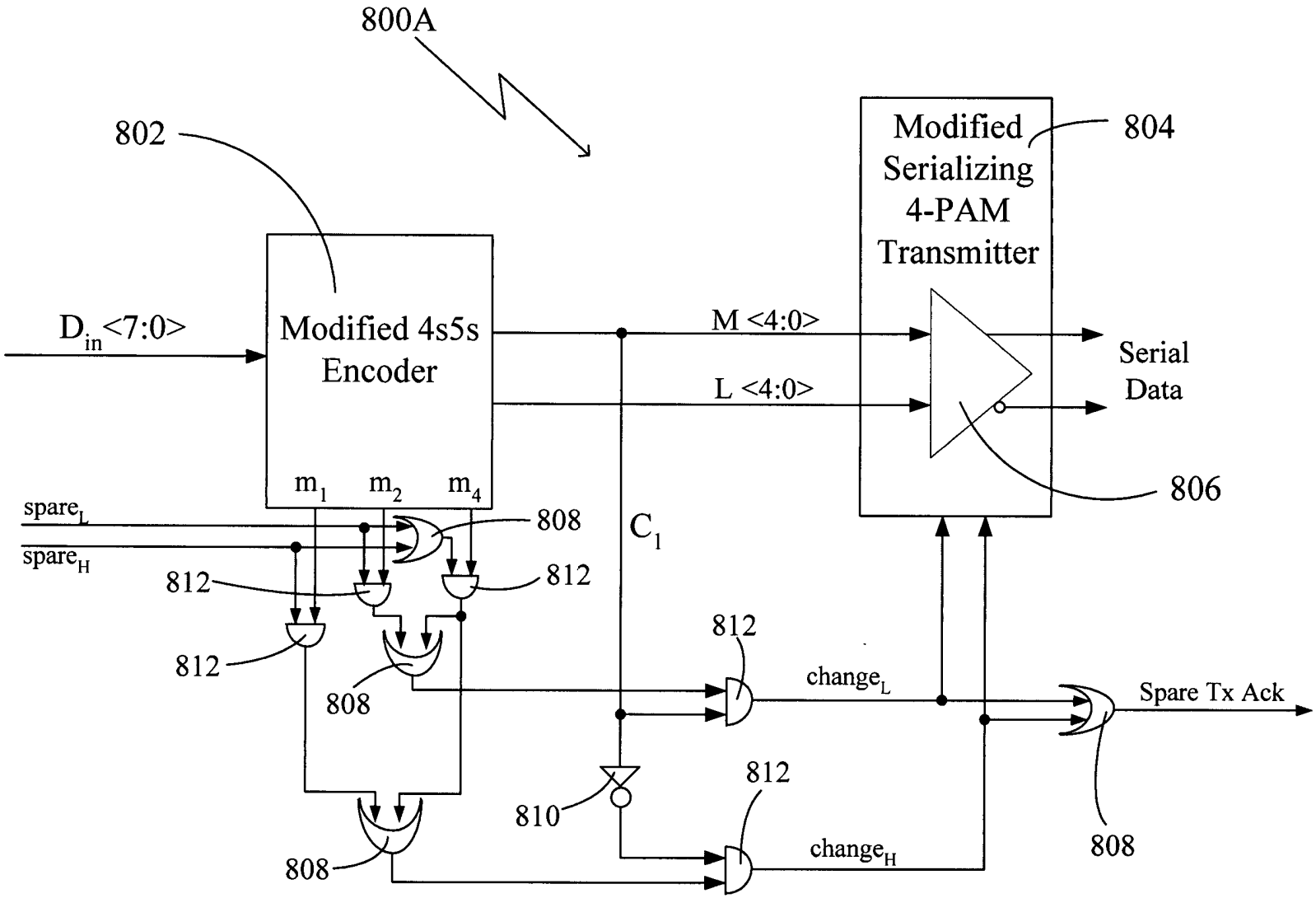
800A
802
Modified 4s5s Encoder
804
Modified Serializing 4-PAM Transmitter
D_{in}<7:0>
M <4:0>
L <4:0>
Serial Data
806
m_1
m_2
m_4
$spare_L$
$spare_H$
808
812
C_1
$change_L$
$change_H$
Spare Tx Ack
810

Figure 8A

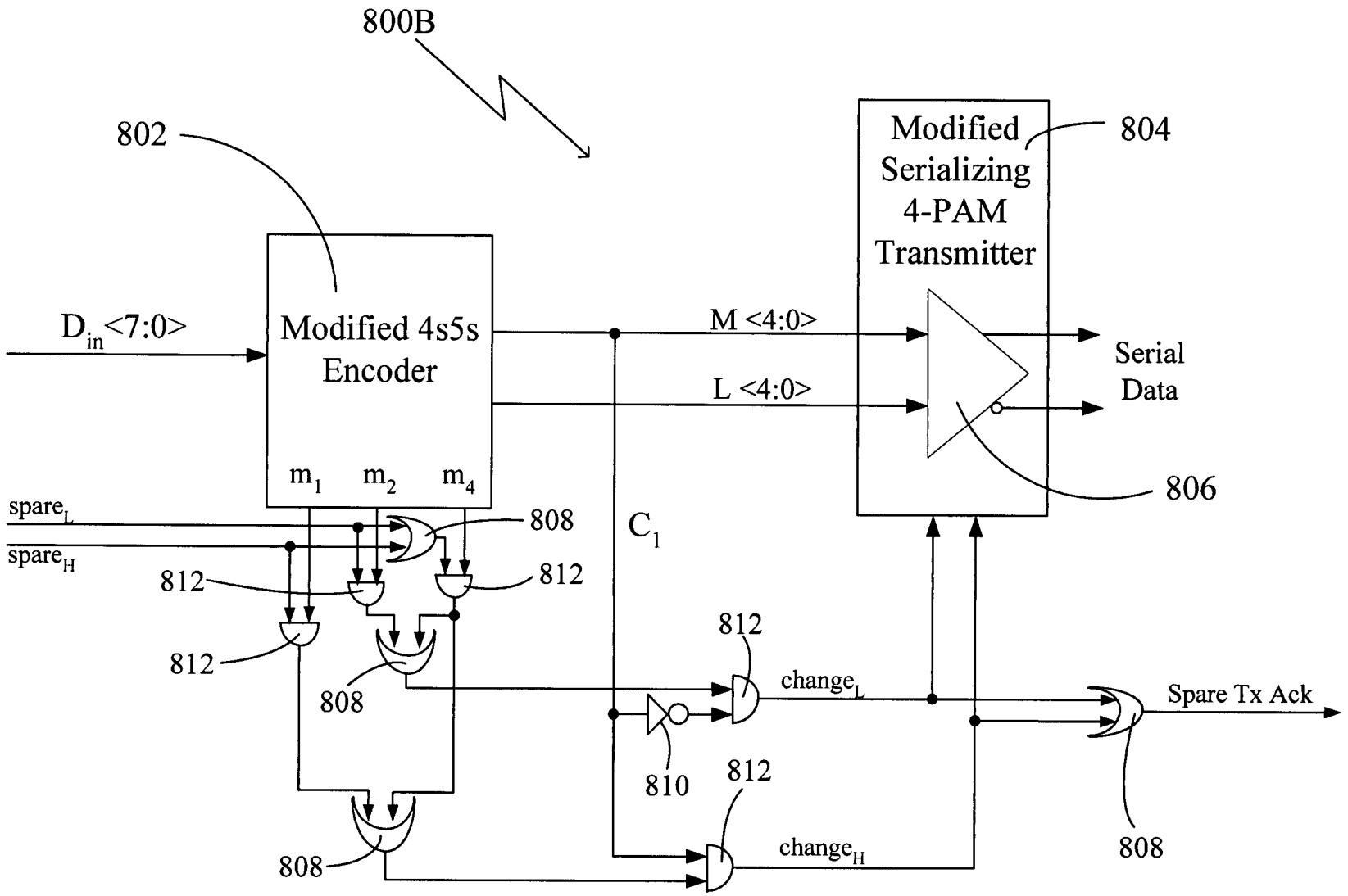
800B
802
Modified 4s5s Encoder
D_{in}<7:0>
m_1 m_2 m_4
Modified Serializing 4-PAM Transmitter
804
M <4:0>
L <4:0>
Serial Data
806
C_1
$spare_L$
$spare_H$
808
812
$change_L$
$change_H$
810
Spare Tx Ack

Figure 8B

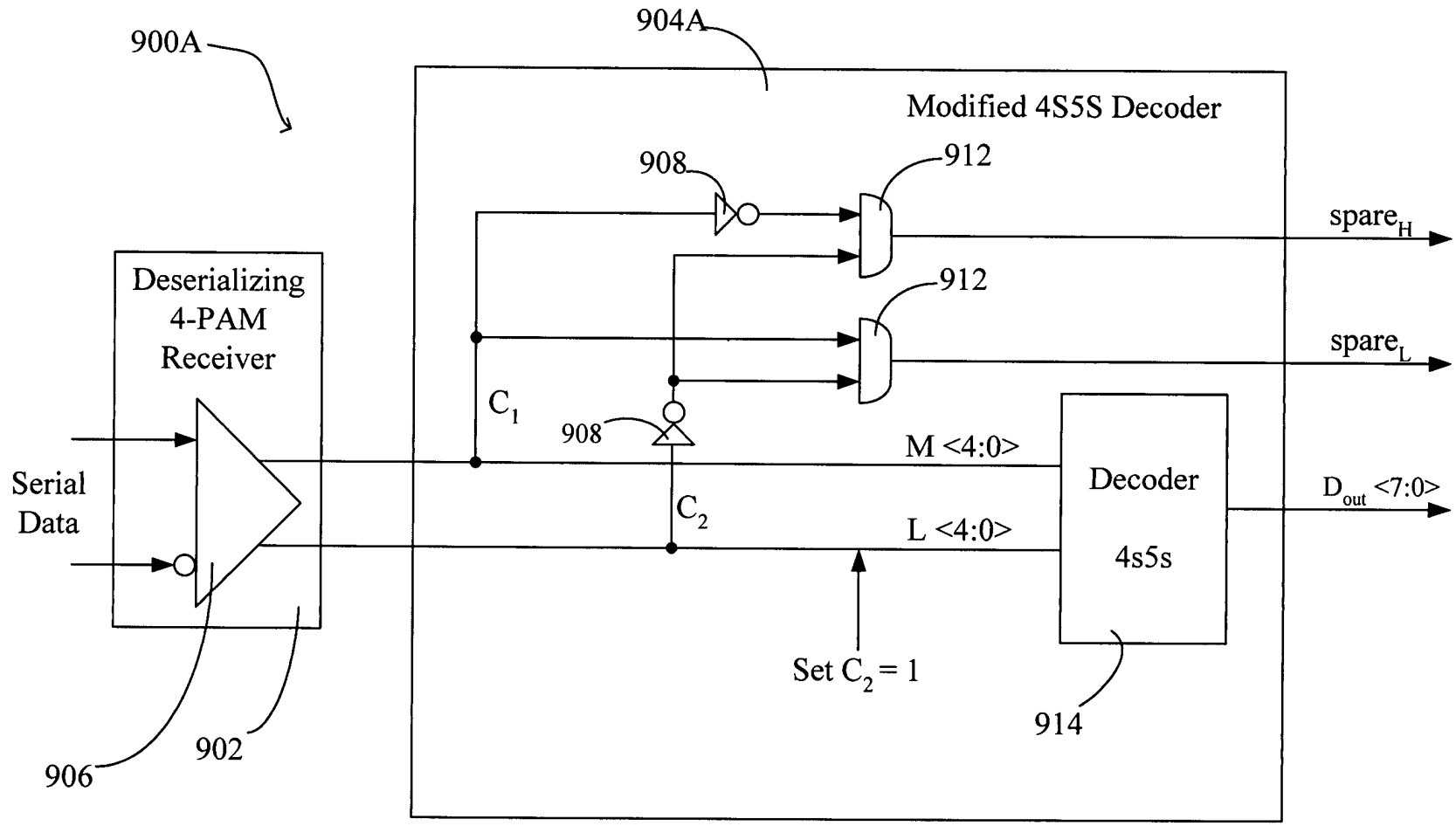
900A
904A
Modified 4S5S Decoder
908
912
912
spare$_H$
spare$_L$
Deserializing
4-PAM
Receiver
C_1
908
M <4:0>
Decoder
4s5s
D_{out} <7:0>
Serial
Data
C_2
L <4:0>
Set C_2 = 1
914
906
902

Figure 9A

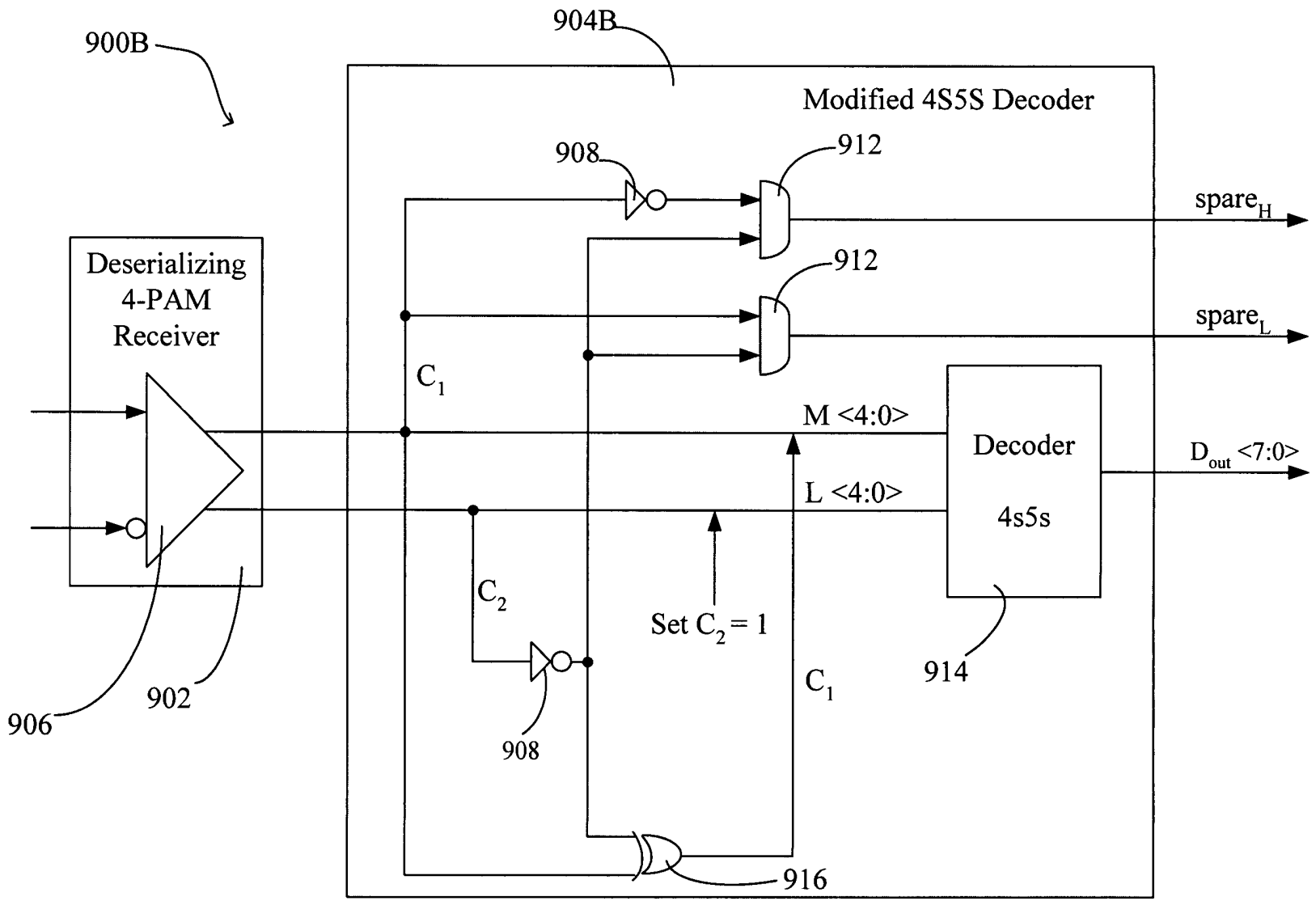
900B
904B
Modified 4S5S Decoder
908
912
912
spare$_H$
spare$_L$
Deserializing
4-PAM
Receiver
C_1
M <4:0>
L <4:0>
Decoder
4s5s
D_{out} <7:0>
C_2
Set C_2 = 1
C_1
914
906
902
908
916

Figure 9B

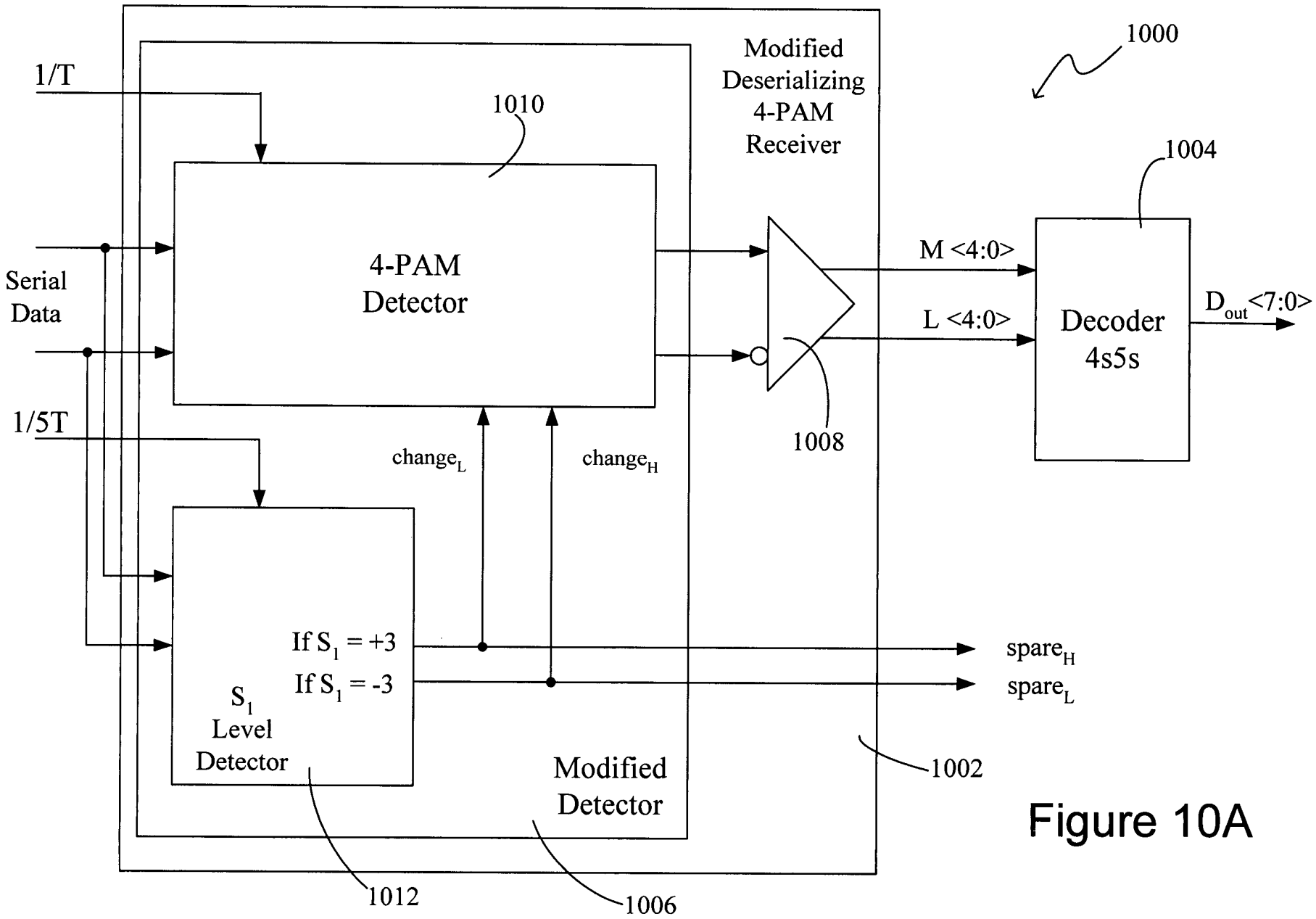
1000
Modified
Deserializing
4-PAM
Receiver
1/T
1010
1004
4-PAM
Detector
Serial
Data
M <4:0>
L <4:0>
Decoder
4s5s
D_{out}<7:0>
1/5T
1008
$change_L$
$change_H$
If S_1 = +3
If S_1 = -3
S_1
Level
Detector
$spare_H$
$spare_L$
1002
Modified
Detector
1012
1006

Figure 10A

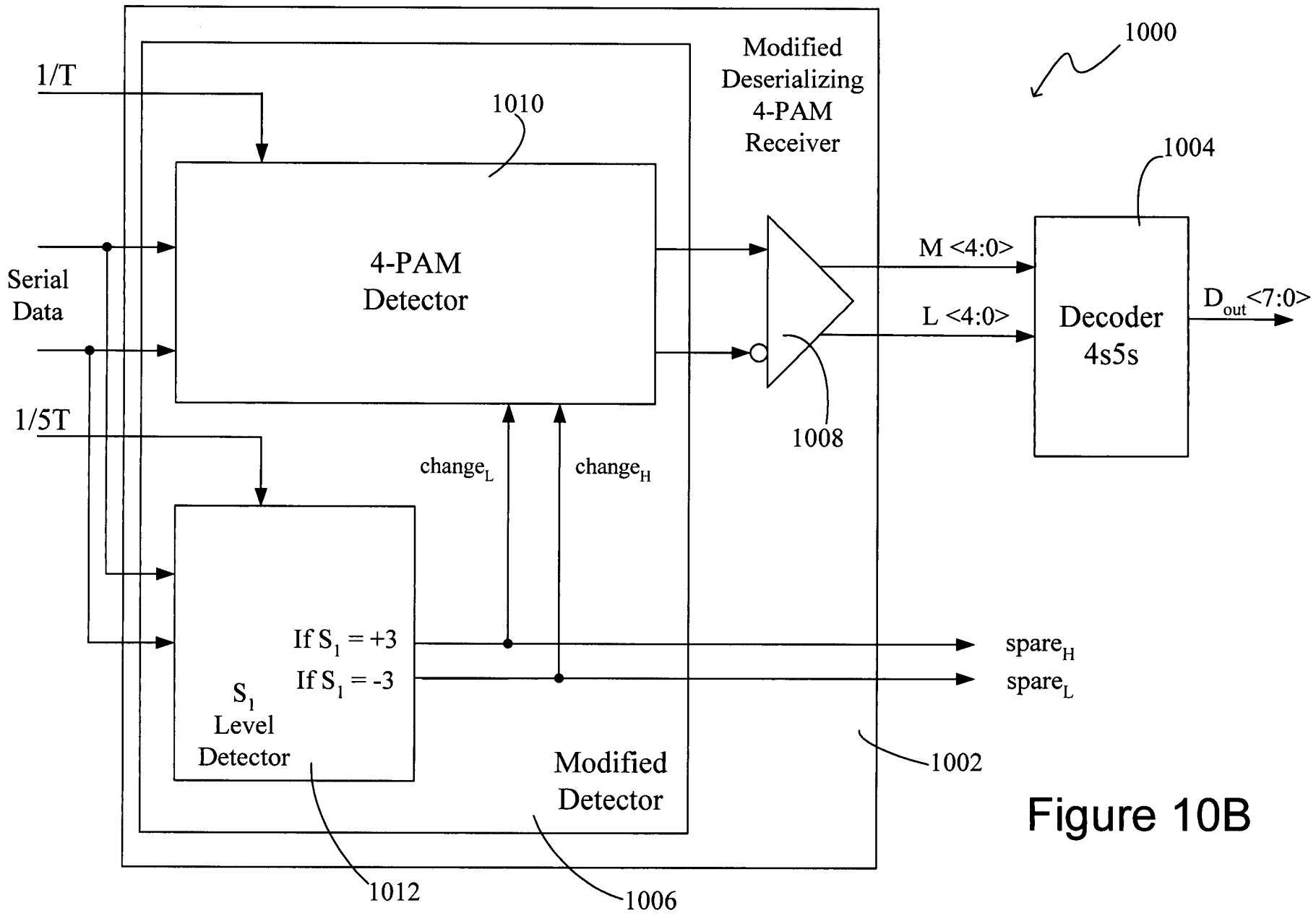
1000
Modified
Deserializing
4-PAM
Receiver
1/T
1010
1004
4-PAM
Detector
Serial
Data
M <4:0>
L <4:0>
Decoder
4s5s
D_{out}<7:0>
1/5T
1008
$change_L$
$change_H$
If S_1 = +3
If S_1 = -3
S_1
Level
Detector
$spare_H$
$spare_L$
1002
Modified
Detector
1012
1006

Figure 10B

Error Detection

Symbol Domain

$[(\text{Case I} \;\&\; (S_1^{(k+1)} = -3)] \text{ OR } [(\text{Case II} \;\&\; (S_1^{(k+1)} = 3)] \text{ OR } [\text{Case III} \;\&\; (S_1^{(k+1)} = \pm 3)]$ → Error Detected

where Case III: $[(S_5^{(k)} = 3) \;\&\; (S_2^{(k+1)} = -3)] \text{ OR } [(S_5^{(k)} = -3) \;\&\; (S_2^{(k+1)} = 3)]$

Bit Domain

$[\text{Case I} \;\&\; (C_1^{(k+1)} = 1) \;\&\; (C_2^{(k+1)} = 0)] \text{ OR } [\text{Case II} \;\&\; (C_1^{(k+1)} = C_2^{(k+1)} = 0)] \text{ OR } [\text{Case III} \;\&\; (C_2^{(k+1)} = 0)]$ → Error Detected

where Case III: $[(C_9^{(k)} = C_{10}^{(k)} = C_4^{(k+1)} = 0) \;\&\; (C_3^{(k+1)} = 1)] \text{ OR } [(C_9^{(k)} = 1) \;\&\; (C_{10}^{(k)} = C_3^{(k+1)} = C_4^{(k+1)} = 0)]$

Figure 11

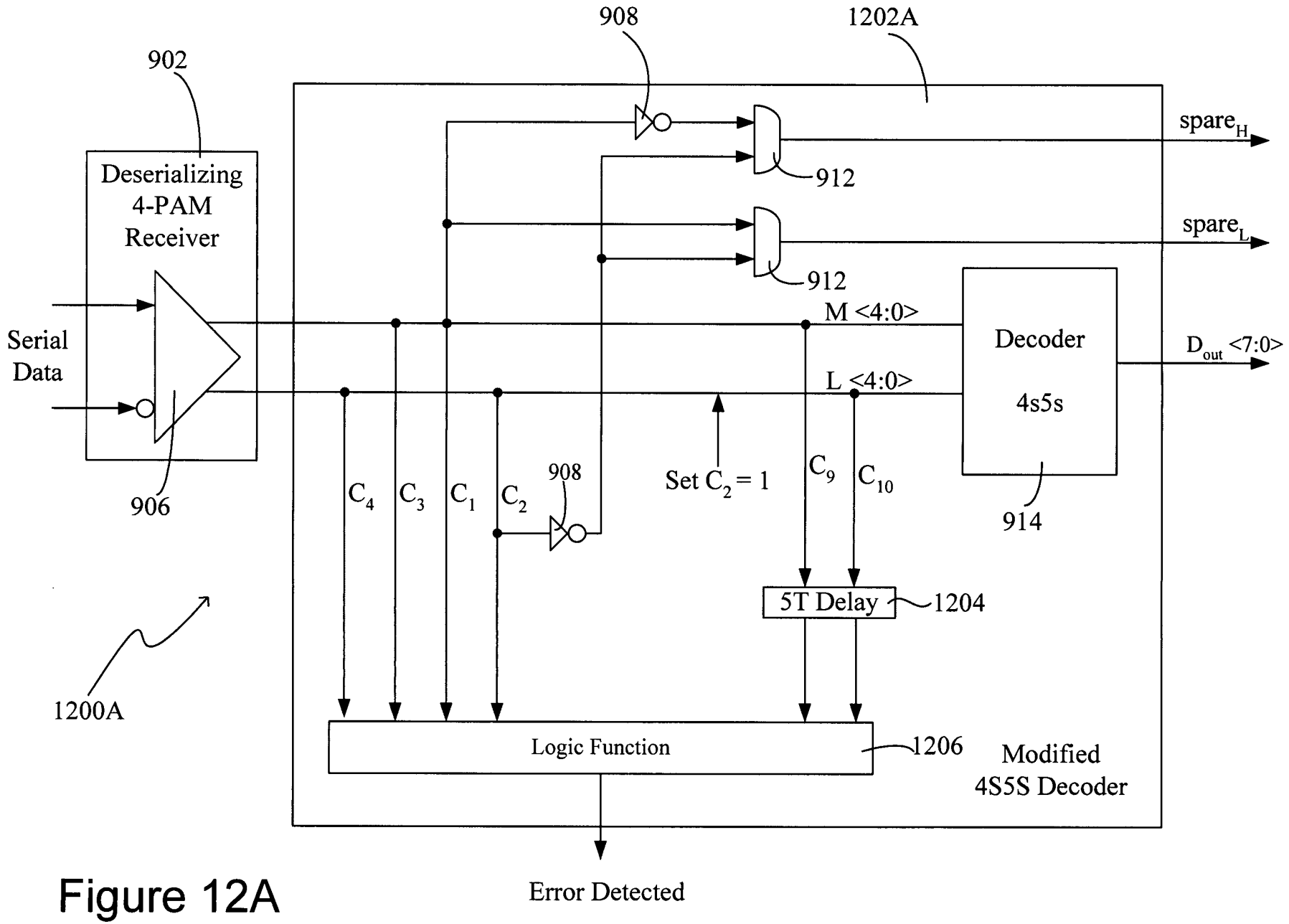
908
1202A
902
Deserializing
4-PAM
Receiver
spare$_H$
912
spare$_L$
912
M <4:0>
Decoder
4s5s
D$_{out}$ <7:0>
Serial
Data
L <4:0>
906
C$_4$
C$_3$
C$_1$
C$_2$
908
Set C$_2$ = 1
C$_9$
C$_{10}$
914
5T Delay
1204
1200A
Logic Function
1206
Modified
4S5S Decoder
Error Detected

Figure 12A

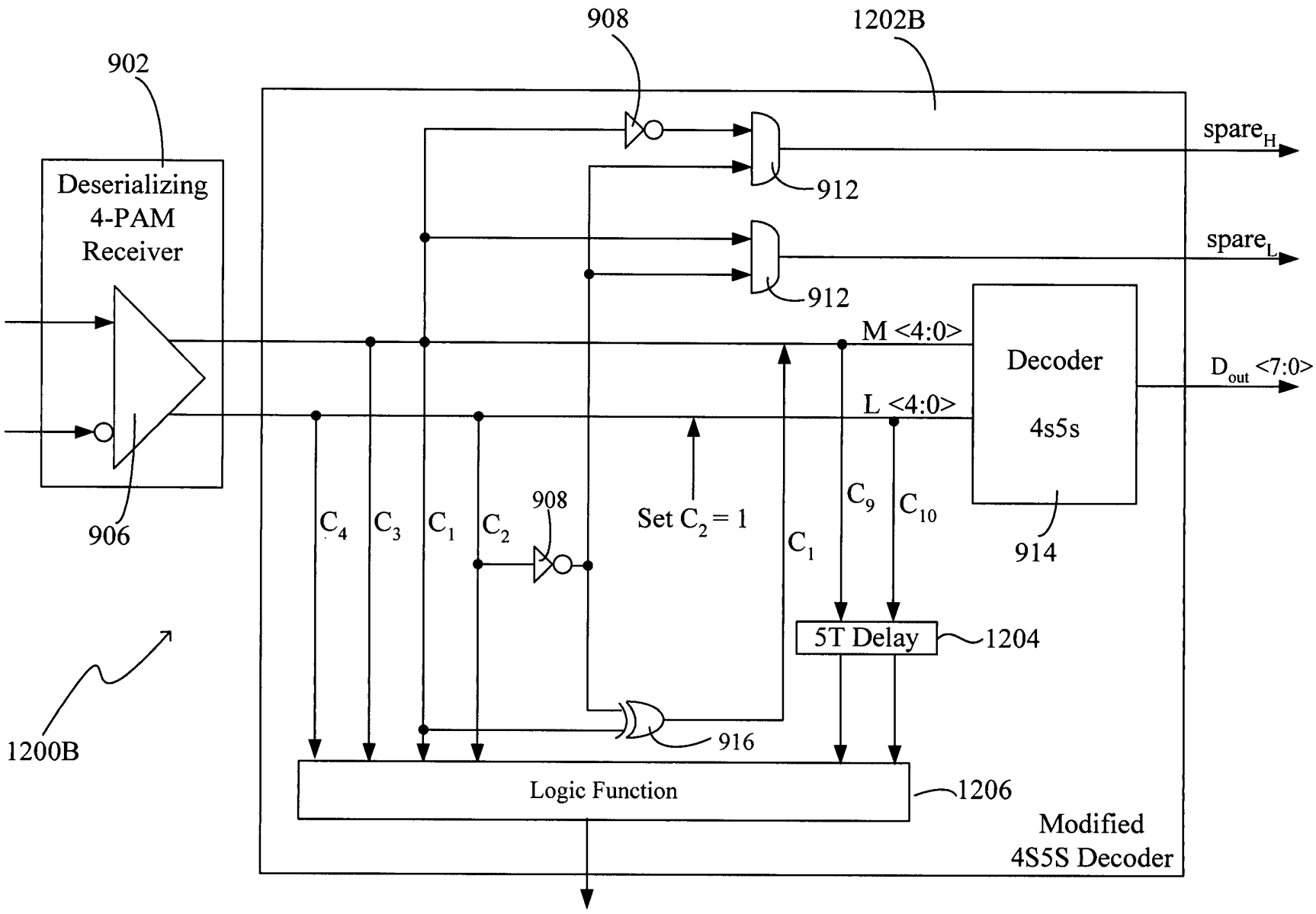
908
1202B
902
Deserializing
4-PAM
Receiver
spare$_H$
912
spare$_L$
912
M <4:0>
Decoder
4s5s
D_{out} <7:0>
L <4:0>
906
C_4
C_3
C_1
C_2
908
Set C_2 = 1
C_1
C_9
C_{10}
914
5T Delay
1204
1200B
916
Logic Function
1206
Modified
4S5S Decoder
Error Detected

Figure 12B